## AMENDMENTS TO THE CLAIMS

1. (Currently amended) A data storage device comprising:

non-volatile memory; and

a read circuit for performing multi-sample read operations on the memory during a normal mode of operation, the read circuit including a digital counter for storing an n-bit count, where n>1, the digital counter having an output that indicates only a single bit of the count;

the read circuit allowing test clock pulses to be applied to the digital counter during a test mode of operation;

whereby the test clock pulses can be counted to determine a state of the digital counter.

2. (Original) The device of claim 1, wherein the read circuit further includes a digital sense amplifier for performing the multi-sample read operations, an output of the digital sense amplifier connected to an input of the digital counter during the normal mode of operation.

3. (Original) The device of claim 2, wherein the performing a multi-sample read operation includes using the digital sense amplifier to take a first sample and cause a state of the digital counter to represent the result of the first sample; using the digital sense amplifier to establish a reference count, and making a comparison of the digital counter state to the reference count.

4. (Original) The device of claim 3, wherein the read circuit further includes a sample/hold for shifting the digital counter state between the sample/hold and the digital counter, and for inverting the sign of its state.

5. (Currently amended) The device of claim 2, wherein the digital sense amplifier includes an integrator for integrating a charge at a rate that is dependent upon a logic value [[store]] stored in a selected memory device; and wherein the state of the digital counter is changed at a rate that is proportional to the integration time.

6. (Currently amended) The device of claim 1, wherein the single bit is a sign-bit of the ~~digital~~ count.

7. (Original) The device of claim 1, wherein the non-volatile memory includes a resistive cross point array of memory cells.

8. (Original) The device of claim 1, wherein the non-volatile memory includes an MRAM array.

9. (Original) A read circuit for a memory device, the circuit comprising:

first means for performing a multi-sample read operation on the memory device, the first means including a digital counter, an output of the digital counter indicating a sign-bit; and

second means for allowing contents of the digital counter to be determined by an external device at least one of during and after the multi-sample read operation.

10. (Original) A method of using a memory device, the method comprising:

performing a multi-sample read operation on the memory device; the multi-sample read operation including a plurality of sense operations on the memory device, a digital counter used during the multi-sample read operation to generate a running sum of values, each value representing a resistance that was sensed during one of the sense operations; and

determining the state of the digital counter during or after the multi-sample read operation, wherein determining the state includes sending clock pulses to an input of the digital counter until a change in a sign-bit of the digital counter, and counting the clock pulses that were sent to the digital counter.

11. (Original) The method of claim 10, wherein the digital counter state is determined prior to completion of the multi-sample read operation, whereby the state indicates a read access time.

12. (Original) The method of claim 10, wherein the digital counter state is determined after the multi-sample read operation has been performed, whereby the state indicates a margin.

13. (Original) The method of claim 10, wherein performing a multi-sample read operation includes taking a first sample of the memory device and causing a state of the digital counter to represent the result of the first sample; using the memory device to establish a reference count, and making a comparison of the reference count and the result of the first sample.

14. (Original) The method of claim 13, wherein each sample includes a sense operation, each sense operation performed by integrating a charge at a rate that is dependent upon a logic value store in the memory device; and using the digital counter to measure the integration time.

15. (Original) A system comprising:

a data storage device including a resistive cross point array of memory cells, and a read circuit operable in normal and test modes of operation, the read circuit including a digital sense amplifier for performing multi-sample read operations on selected memory cells of the array during the normal mode and a digital counter for storing results of the multi-sample read operations, an output of the digital counter providing a sign-bit;

a memory tester including a source for generating test clock pulses, a circuit for determining when the sign-bit changes, and a counter for counting the test clock pulses until the sign-bit changes.

the read circuit allowing the test clock pulses to be applied to the digital counter during the test mode of operation.

16. (Currently amended) Apparatus for externally testing a non-volatile memory device including a digital counter, the counter having an input and an output, the output indicating only a sign-bit, the apparatus comprising:

means for supplying test clock pulses to the input of the counter;

means for examining the output of the digital counter to determine when the sign-bit changes;

means for counting a number of test clock pulses supplied to the counter input, the count being stopped when the sign-bit changes; and

means for using the count of test clock pulses to determine a performance parameter of the non-volatile memory.

17. (Original) The method of claim 16, wherein a binning function is performed by the means for using the count.

18. (New) The device of claim 1, further comprising a digital sense amplifier and means for connecting an output of the digital sense amplifier to an input of the digital counter during the normal mode of operation, the means disconnecting the output of the digital sense amplifier and instead allowing an external source to supply the test clock pulses to the input of the digital counter during the test mode of operation.